



WISHING YOU A HAPPY AND PROSPEROUS NEW YEAR 2005

CIR-Q-TECH at Electronica 2004, Munich.



**CIR-Q-TECH TAKO TECHNOLOGIES PVT. LTD.,
Had the privilege of presenting its products
courtesy CBI, Amsterdam, at Electronica 2004
exhibition held at Munich During 9-12th November.**

Highlights During 2004

- ❖ CIR-Q-TECH is Audited and Approved by Center for promotion of imports from developing countries, Government of Netherlands as a prospective exporter of its products to the European community.
- ❖ CIR-Q-TECH obtains CE marking for some of its test instruments.
- ❖ CIR-Q-TECH secures one-year contract for holding Seminars for ISRO engineers and scientists.
- ❖ CIR-Q-TECH Exhibits products at Electronica 2004, Munich.
- ❖ CIR-Q-TECH secures first order for export of its ESD Laminates.
- ❖ CIR-Q-TECH is authorized by M/S Forbo, Switzerland and M/S Bolidt for marketing their internationally known ESD Flooring materials.
- ❖ CIR-Q-TECH is honored to be one of the top 5 chosen by International Facilitation Managers Association, in the category, " Innovative Solutions".
- ❖ CIR-Q-TECH enters project consultancy services by taking up contractual work for Larsen and Toubro, Mysore and Lensel Optics, Pune.

ESD COMPATIBLE FLOORING SYSTEMS

CIR-Q-TECH TAKO TECHNOLOGIES PVT. LTD., introduces ESD compatible flooring systems manufactured by M/S Bolidt Top Synthetics, Netherlands.

There are several types of this flooring eg. Bolidt top 525-stato compound; Bolidt top E.Lo 20345 etc. Bolidt top 525 stato compound forms the top layer of a Bolidt top525 stato system and consists of 3 components based on solvent free synthetic resins to which inert fillers are added. Shortly before the application the components must be mixed to a smooth homogeneous mass.



Properties:

1. After complete curing Bolidt top 525-stato system forms a universal conducting floor surface complies with such standards as EM1081, NFPA56A, EOS/ESD, and Draft Std7.1 etc.
2. Density 1.5 Kg/Cubic Meter.
3. Skid resistance : 99 dry, 31 wet.
4. Electrical Characteristics: $>5 \times 10^4$ & $< 5 \times 10^7$ ohms. For explosive areas it will be $> 5 \times 10^4$ & $< 5 \times 10^6$ ohms.
5. Colours: Bolidt stato compounds are available in several colours.

Bolidt top 525 stato compound has good resistance to chemicals, wear and impact and has excellent adhesion to cement bound substrates.

The Bolidt top system can be suitably adapted to form a flooring system required by such different industries as

1. Chemical and petrochemical Industries
2. Heavy & metal industry.
3. Electronics & High tech industry
4. Pharmaceutical industry
5. Printing and paper industry
6. Automobile industry
7. Food industry
8. Synthetic Sports Floor systems
9. Civil & Rail Systems (Bridges, Flyovers, runways, Platforms)

Bolidt systems can also be used in the public buildings like schools, Theatres, Supermarkets etc.

New Methods for the Assessment of ESD Threats to Electronic Components

Jaakko Paasi , Jeremy Smallwood, Hannu Salmela

Continued from 2nd issue:

III. Proposal of a Discharge Current Threshold for ESD Damage

A. Derivation of the Current Threshold

For ESD damage to occur with intermediate or long ESD pulse durations, the internal power dissipation in the weak region must exceed a threshold value to overcome heat losses from the region. This power dissipation must occur at some discharge current level, and a current threshold for ESD damage therefore is proposed. Many workers have assessed ESD damage to components on the basis of the non-adiabatic Wunsch-Bell equation. This can be justified for

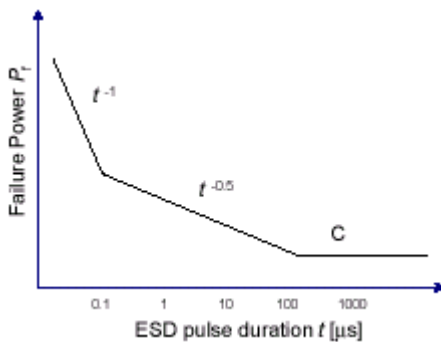


Figure 2: Device failure power vs. ESD pulse duration: a simplified model for energy susceptible devices. ESD pulse durations for the different regimes are just examples and can, in practice, greatly differ from the values given in the figure.

intermediate duration ESD events. The middle term of Eq. (3) can be combined with the device model, Eq. (1) leading to

$$P_f = I_{\text{end}}^2 R_d + I_{\text{end}} V_{\text{bd}} = S \left[\sqrt{\pi K \rho C_p} \right] \Delta T t^{-0.5} \quad (4)$$

All the device parameters S , K , \tilde{n} , c_p and T_{ref} , r_d , v_{bd} are dependent on device construction and may, to a first approximation, be assumed to be constants for a given device and failure mechanism. Equation (4) contains the information required for the calculation of the current threshold for damage, but it cannot be easily solved for the current. The situation, however, is simplified if we take into account typical damage mechanisms of energy sensitive devices. In reverse biased junction burnout, v_{bd} is typically much higher than $v_{\text{esd},r,d}$ [7] and Eq. (4) could be simplified by approximating the term $v_{\text{esd},r,d}$ to be negligible. In metallization burnout, on the other hand, $v_{\text{esd},r,d} \gg v_{\text{bd}}$ [7] and the second term in Eq. (4), $v_{\text{esd},r,d}$, is negligible. This simplification lets us to derive current thresholds for failure and to get limits for the dependence of the failure current on the ESD duration. For low ESD current levels associated with low HBM

ESD device withstand voltages and for ESD failures due to junction burnout, we can assume that $V_{bd} \gg V_{td}$ and power dissipation is mainly across the device junction. Then Eq. (4) can be approximated by

$$P_f = I_{esd} V_{bd} = S \left(\sqrt{\pi K \rho C_p} \right) \Delta T t^{-0.5} \quad (5)$$

This gives a failure current threshold I_f of

$$I_f = G t^{-0.5} \quad (6)$$

where G is approximately constant for a given device and failure mode

$$G = \frac{S \left(\sqrt{\pi K \rho C_p} \right) \Delta T}{V_{bd}} \quad (7)$$

If this current level is exceeded, the power dissipation will rapidly exceed the power required to heat the damage site to the damage temperature ($P=f(T)$) and, providing the discharge is of sufficient duration, damage will occur. An ESD event having a lower peak current can be expected to not exceed the power threshold, and therefore not cause damage. A threshold obtained for a longer duration discharge, where power loss from the heated region is significant, can be expected to give a safe value for shorter ESD durations.

If the ESD failure mode is such that $V_{bd} \ll V_{td}$, like in ESD failures due to metallization burnout, Eq. (4) can be approximated by

$$P_f = I_{esd}^2 R_d = S \left(\sqrt{\pi K \rho C_p} \right) \Delta T t^{-0.5} \quad (8)$$

In this case the threshold could be written as

$$I_f = \sqrt{G} t^{-0.25} \quad (9)$$

This solution may also suit certain types of resistive device such as GMR heads. It is less severe a derating function than the $t^{-0.5}$ relation. One question is, how can the threshold I_f be obtained? We do not generally know the characteristics of the weakest region in the device, or parameters such as size or effective device resistance. We can solve this problem empirically by turning to standard ESD test data from the HBM model to give a reference point on the failure curve. In the HBM ESD withstand test the discharge current is primarily governed in most cases by the series 1500 Ω resistance, R_{HBM} . The duration of the discharge is about 150 ns, which is likely to be within the non-adiabatic heating regime. We can propose that the peak current in the HBM ESD event may directly give a reasonable measure of the ESD current threshold for damage of the device in HBM-like situations. Perhaps most usefully, the test is already performed on the majority of devices. If the voltage dropped across the device is small the device HBM withstand voltage V_{HBM} can be considered dropped across the HBM circuit series resistor, and the peak ESD current threshold I_{fHBM} can be calculated from

$$I_{fHBM} = \frac{V_{HBM}}{R_{HBM}} \quad (10)$$

where $R_{HBM} = 1500 \Omega$. Thus a threshold of 100 V HBM gives a peak current threshold of 66.7 mA. Protection of 10 V HBM devices requires a reduction in peak current threshold to 6.7 mA. In general, the allowable current is 0.67 mA per Volt HBM withstand. The failure current threshold can be expected to be valid for exponentially decaying waveforms of durations similar to the HBM pulse $t_{HBM} = 150$ ns. The advantage of this approach is that we need to know nothing about

the internal structure of the device, except to confirm that it is subject to energy related failure rather than being a voltage sensitive type. The HBM test gives us a point on the threshold I/t curve. If necessary we can derate the current to give safe working at other ESD pulse durations.

To be Continued...

Seminars were arranged outside the ESD School, Electronic City at the following locations

- **DRDO**, Hyderabad.
- **Texas Instruments** , Bangalore.
- **BPL**, Bangalore
- For **ISRO**, Bangalore, (Exclusively at our ESD School)

The following Surveys / Audits were conducted by the ESD training Division

- **Texas Instruments**, Bangalore.
- **GE Medical Systems**, Bangalore.
- **Sun Fiber Optics**, Cochin.
- **Intel Technologies**, Bangalore.
- **Cisco Systems**, Bangalore.